AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of automatically inserting antenna diodes for an integrated circuit design, comprising:

selecting a block of standard cells defining at least a portion of the integrated circuit design;

associating a diode circuit with at least one input port of said block of standard cells ~~to form an augmented block; and~~;

laying out components of said block of standard cells and said diode circuit associated with each said at least one input port; and

routing conductors for connecting said components and connecting each said at least one input port to said associated diode circuit.

~~implementing said augmented block within said integrated circuit design.~~

Claim 2. Cancelled.

3. (Currently Amended) The method of claim [[2]] 1, wherein said diode circuit associated with each said at least one input port comprises a standard cell selected from said cell library.

4. (Original) The method of claim 3, further comprising:

creating placement constraint data for said diode circuit associated with said at least one input port.

5. (Original) The method of claim 4, wherein said laying out step comprises placing said diode circuit associated with said at least one input port in accordance with said placement constraint data.

6. (Currently Amended) The method of claim 5, further comprising:

responsive to said ~~implementing step~~ steps of laying out and routing, identifying an antenna violation associated with an offending input port of said at least one input

port;

associating at least one additional diode circuit with said offending input port to form an augmented block; and

re-implementing said augmented block within said integrated circuit design.

7. (Original) The method of claim 6, further comprising repeating said identifying step, said associating at least one additional diode step, and said re-implementing step a plurality of times.

8. (Original) The method of claim 6, wherein said re-implementing step comprises:

replacing at least one filler cell of said augmented block with said at least one additional diode circuit.

9. (Original) The method of claim 6, wherein said identifying step comprises:

determining a ratio of an area of a conductor associated with said offending input port to an area of a gate of a transistor associated with said offending input port; and

comparing said ratio to a threshold.

10. (Currently Amended) The method of claim 1, further comprising:

responsive to said ~~implementing step~~ steps of laying out and routing, identifying an antenna violation associated with an offending input port of said at least one input port;

associating at least one additional diode circuit with said offending input port to form an augmented block; and

re-implementing said augmented block within said integrated circuit design.

11. (Original) The method of claim 1, wherein said at least one input port comprises all input ports of said block.

12. (Currently Amended) An apparatus for automatically inserting antenna diodes for an integrated circuit design, at least a portion of the integrated circuit being defined by a block of standard cells selected from a cell library, the apparatus comprising:

means for associating a diode circuit with at least one input port of said block of standard cells ~~to form an augmented block; and~~;

means for laying out components of said block of standard cells and said diode circuit associated with each said at least one input port; and

means for routing conductors for connecting said components and connecting each said at least one input port with said associated diode circuit.

~~means for implementing said augmented block within said integrated circuit design.~~

13. (Currently Amended) The apparatus of claim 12, further comprising:

means for identifying an antenna violation associated with an offending input port of said at least one input port ~~responsive to said implementing means~~;

means for associating at least one additional diode circuit with said offending input port to form an augmented block; and

means for re-implementing said augmented block within said integrated circuit design.

14. (Original) A method of forming an integrated circuit, comprising:

associating a diode circuit with each of a plurality of primary input ports of an embedded logic circuit defining at least a portion of the integrated circuit, a remaining portion of the integrated circuit defining existing logic circuitry;

laying out components of said embedded logic circuit;

routing conductors connecting said components; and

integrating said embedded logic circuit with said existing logic circuitry onto a chip to form the integrated circuit.

15. (Original) The method of claim 14, further comprising:

responsive to said integrating step, identifying an antenna violation associated with an offending primary input port of said plurality of primary input ports;

associating at least one additional diode circuit with said offending primary input port; and

re-integrating said embedded logic circuit with said existing logic circuitry onto said chip.

16. (Original) The method of claim 15, wherein said components of said embedded logic circuit, said diode circuit associated with each of a plurality of primary input ports, and said additional diode circuit are composed of standard cells selected from a cell library.

17. (Original) The method of claim 16, further comprising replacing at least one filler cell of said embedded logic circuit with said at least one additional diode circuit.

18. (Original) The method of claim 14, wherein said integrated circuit is a programmable logic device and at least a portion of said existing logic circuitry comprises programmable logic blocks.

19. (Original) The method of claim 18, wherein said embedded logic circuit is a processor.

20. (Withdrawn) A programmable logic device, comprising:

programmable logic;

an embedded logic circuit having a plurality of interconnect lines terminating within said programmable logic; and

at least one diode circuit disposed proximate to a respective at least one interconnect line of said plurality of interconnect lines.

21. (Withdrawn) The programmable logic device of claim 20, wherein each said at least one interconnect line associated with said at least one diode circuit is a primary input port of said embedded logic circuit.